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- Synplify Pro tool to handle timing closure with best in class logic synthesis results, fast runtimes, and good timing correlation.
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February 2021 Overview of the Synthesis Tool This section introduces the technology, main features, and user interface of the FPGA synthesis tool. See the following for details: • ...

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Start->Programs->Synopsys->FPGA Synthesis D-2010.03->Synplify Pro. If you use any other version of the software, results may not exactly match the results in

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the tutorial, although you can still follow the general methodology described in this document. 2. On Linux, type this at the command line: `synplify_pro` The command starts the synthesis tool.

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Synopsys, Inc. January 2014 CHAPTER 1

Introduction This document is part of a set that includes reference and procedural information for the Synopsys® Synplify Pro® FPGA synthesis tools. This document describes the attributes and directives available in the synthesis tools.

1. Start the Synopsys FPGA Synthesis tool (Synplify, Synplify Pro, Synplify Premier, or Certify).
2. In the project view, click the Open Project button to display the Open Project dialog box and click the Existing Project button.
3. Navigate to the tutorial directory where the Identify RTL Debugger is installed.

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using some typical tasks and familiarize
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design is an 8-bit micro controller. After
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design blocks as needed to compose the ideal mix of incremental synthesis and to change that mix at any time during the design process. The designer can choose which blocks of the FPGA can be synthesized independently of each other. The Synplify Pro and Synplify Premier tools treat each

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